WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a multilayered film including a first dielectric film, an etching stopper and a second dielectric film stacked on said semiconductor substrate in this order, the dielectric constant of said etching stopper being larger than that of said first and second dielectric films; and

a metal interconnect formed in said multilayered film;

wherein the upper surface of said etching stopper is located under the upper surface level of said metal interconnect and the under surface of said etching stopper is located over the under surface level of said metal interconnect.

2. The semiconductor device as set forth in Claim 1, wherein the dielectric constant of said etching stopper is less than or equal to 5.

3. The semiconductor device as set forth in Claim 1, wherein the dielectric constant of said etching stopper is larger than or equal to a summation of 2 and the dielectric constant of either one of the dielectric constants of said first and second dielectric films.

4. The semiconductor device as set forth in Claim 2, wherein the dielectric constant of said etching stopper is larger than or equal to a summation of 2 and the dielectric constant of either one of the dielectric constants of said first and second dielectric films.

5. The semiconductor device as set forth in Claim 1, wherein said metal interconnect includes copper as a constituting element.

6. A method of manufacturing a semiconductor device, comprising:

forming a first dielectric film on a semiconductor substrate;

forming an etching stopper that has a higher dielectric constant than said first dielectric film on said first dielectric film;

forming a second dielectric film that has a lower dielectric constant than said etching stopper on said etching stopper;

performing selective etching on said second dielectric film to form a trench until said etching stopper is exposed;

removing said etching stopper exposed at the bottom of said trench until said first dielectric film is exposed;

performing selective etching on said first dielectric film to a predetermined thickness to have the depth of said trench having a predetermined depth; and

forming a metal film in said trench.

7. The method as set forth in Claim 6, further comprising: performing selective etching on said etching stopper and said first dielectric film to form a via hole, after forming said second dielectric film and prior to performing selective etching on said second dielectric film to form a trench, wherein said metal film is formed in said via hole as well.

8. The method as set forth in Claim 6, wherein the dielectric constant of said etching stopper is less than or equal to 5.

9. The method as set forth in Claim 7, wherein the dielectric

constant of said etching stopper is less than or equal to 5.

10. The method as set forth in Claim 6, wherein the dielectric constant of said etching stopper is larger than or equal to the total value of 2 and the dielectric constant of either one of the dielectric constants of said first and second dielectric films.

11. The method as set forth in Claim 7, wherein the dielectric constant of said etching stopper is larger than or equal to the total value of 2 and the dielectric constant of either one of the dielectric constants of said first and second dielectric films.

12. The method as set forth in Claim 6, wherein said metal interconnect includes copper as a constituting element.

13. The method as set forth in Claim 7, wherein said metal interconnect includes copper as a constituting element.

14. The method as set forth in Claim 6, further comprising: performing plasma exposure or UV treatment to improve the surface of said second dielectric film after forming said second dielectric film.

15. The method as set forth in Claim 7, further comprising: performing plasma exposure or UV treatment to improve the surface of said second dielectric film after forming said second dielectric film.

16. The method as set forth in Claim 6, wherein said etching stopper is formed with the surface of said first dielectric film untreated.

17. The method as set forth in Claim 7, wherein said etching stopper is formed with the surface of said first dielectric film untreated.